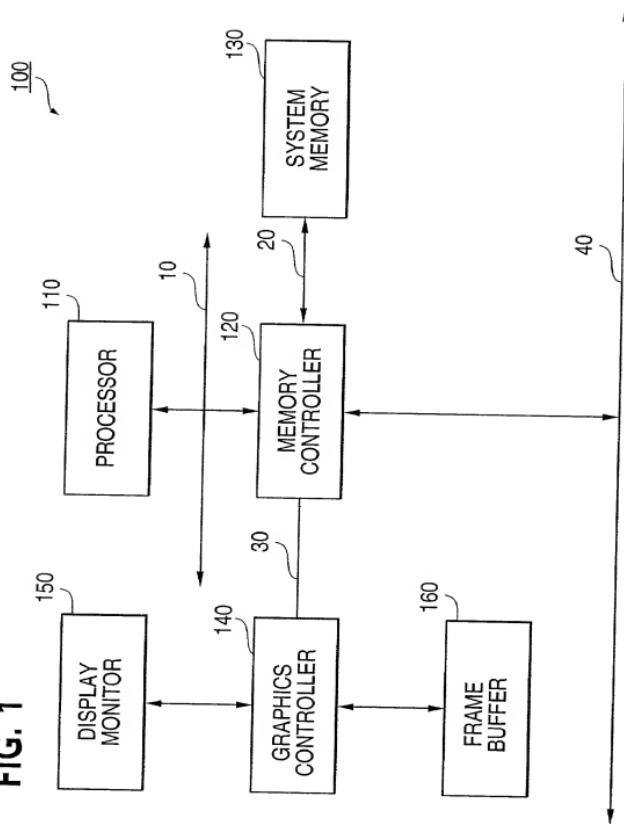
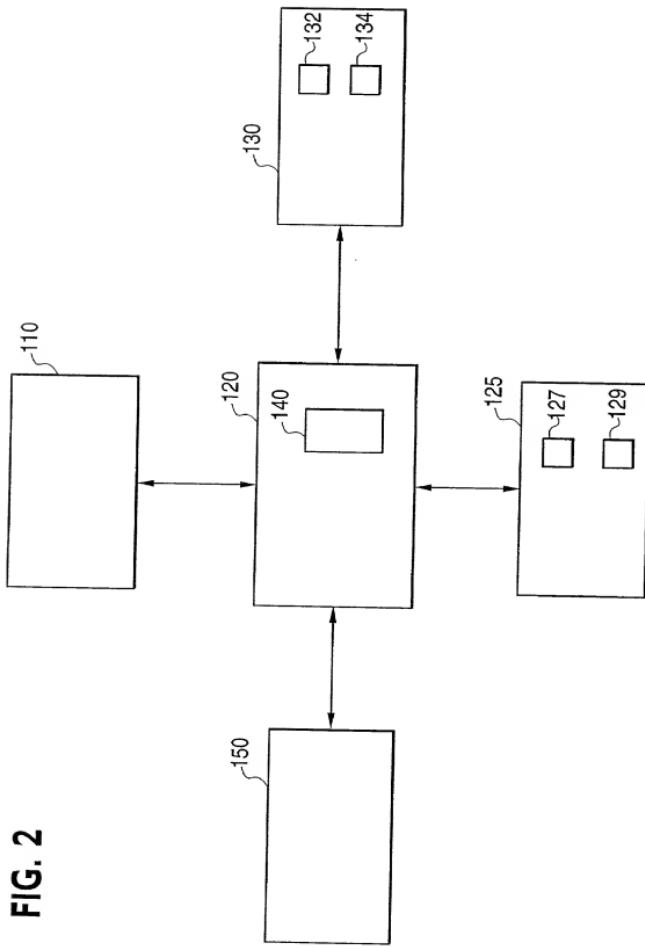


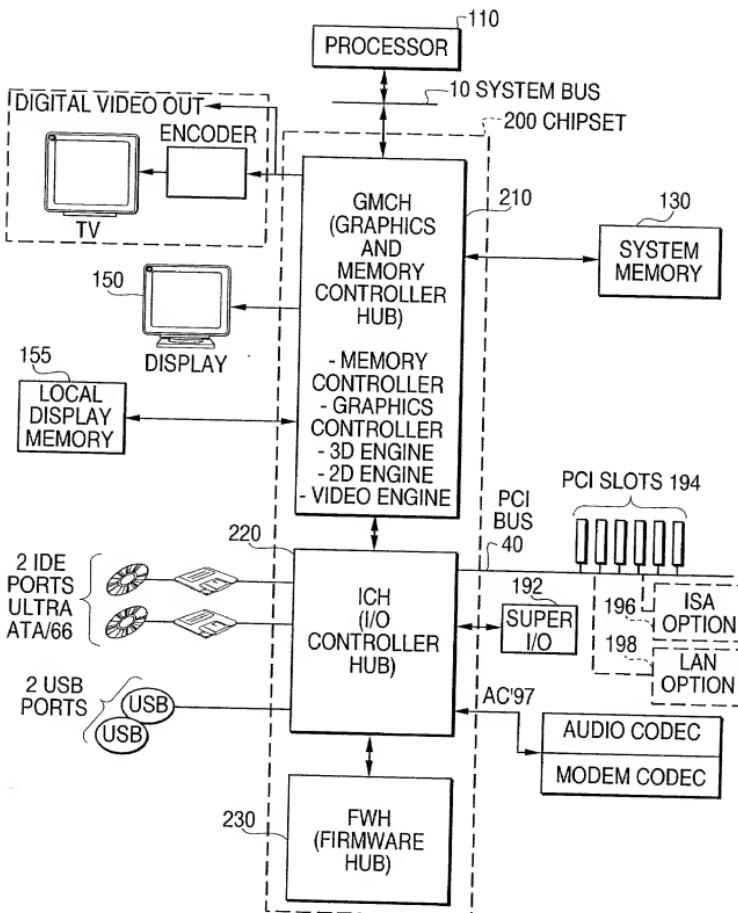
**FIG. 1**



**FIG. 2**

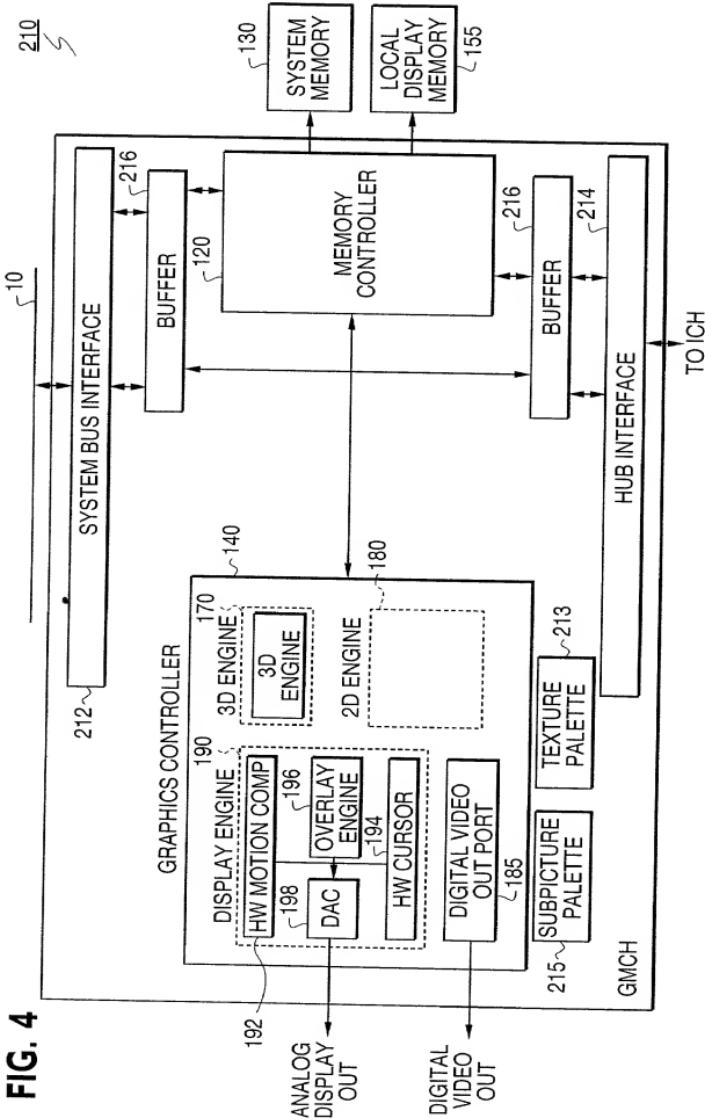


**FIG. 3**

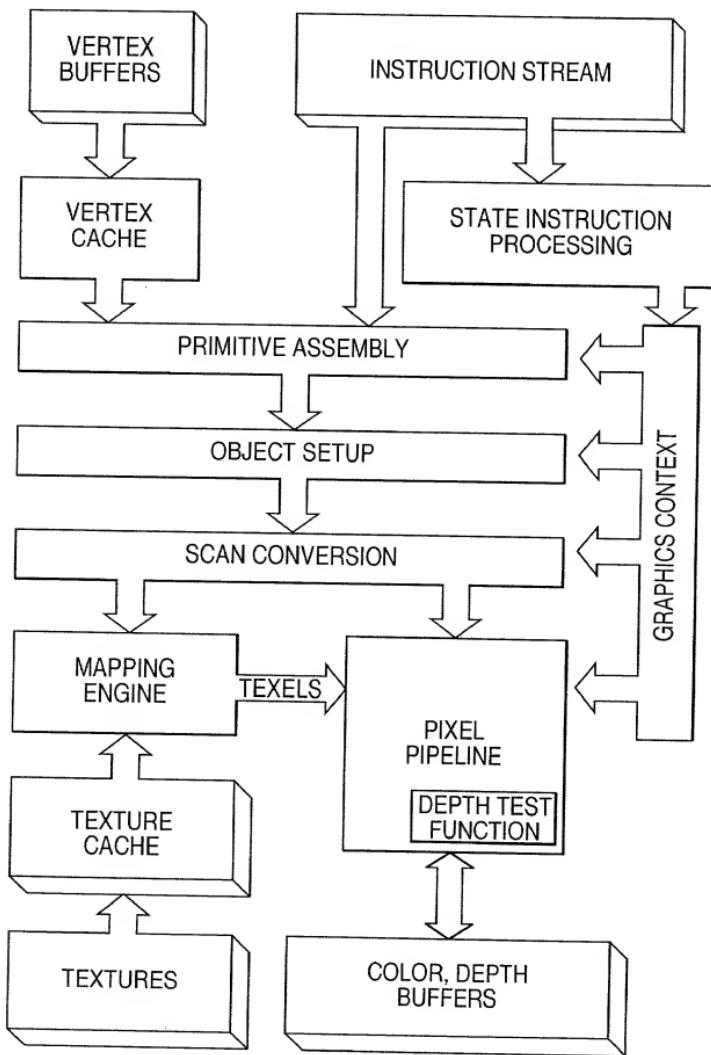


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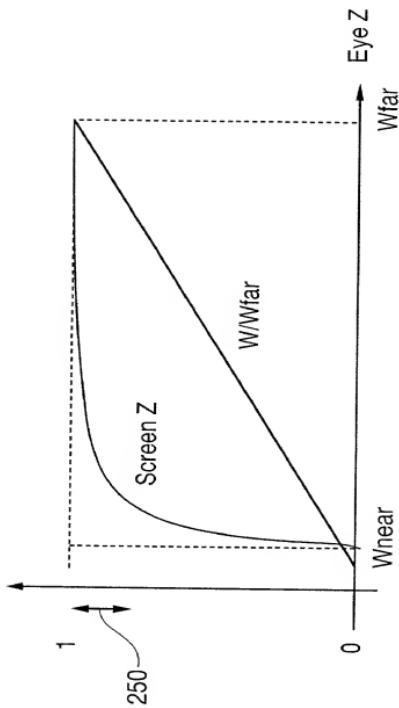
**FIG. 4**



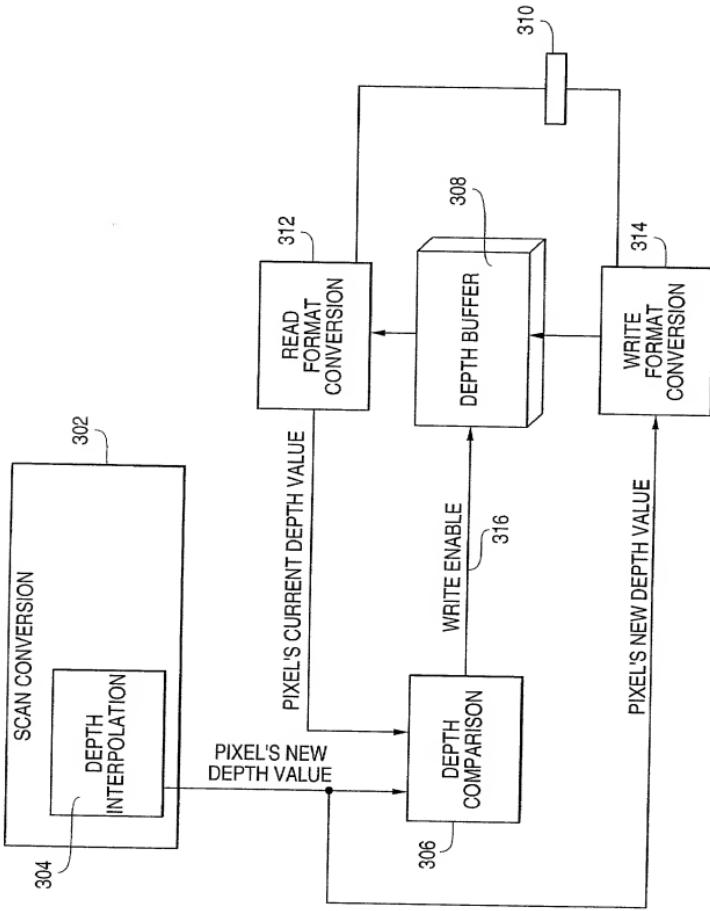
**FIG. 5**



**FIG. 6**



**FIG. 7**



**FIG. 8A**

Bit	Biased Exponent	Description
15:16-n	Biased Exponent:	
15:16-n	Format: n-bit unsigned biased exponent, where n= WExponentSelect. The exponent is biased by $2^n$ .	
15-n:0	Fraction:	(16-n)-bit fractional portion of the floating point significand.

**FIG. 8B**

Bit	Normalized W	Description
15:0	Normalized W (W/Wfar): Format: [0:16] Range = [0,1]	

**FIG. 8C**

Biased Exponent (n bits)	Significand		Represented Value (W/Wfar)
	Integer	Fraction	
$exp = 0.2^{n-1}$	1	frac	$1.\text{frac} * 2^{\exp(2^{n-1})}$

**FIG. 9A**

Bit	Stencil	24	23	24-n	23-n	Fraction
Description						
31:24	Stencil: Format: U8 Range = [0..255]					
23:24-n	Biased Exponent: Format: n-bit unsigned biased exponent, where n= WExponentSelect. The exponent is biased by $2^n$ .					
23-n:0	Fraction: Format: (16-n)-bit fractional portion of the floating point significand.					

**FIG. 9B**

Bit	Stencil	24	23	0	Normalized W
Description					
31:24	Stencil: Format: U8 Range = [0..255]				
23:0	Normalized W (W/W(ar): Format: U0:24 Range = [0, 1]				